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PATENT NUMBER and ISSUE DATE

U.S. UTILITY Patent Application

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ļ	TITLE · Metho	od for fabricating a	metal res	sistor in an IC	chip and re	lated s	structure	
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1	*APPLICANT	S: Kar Roy	Arjun; H	loward David;				
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NOTICE OF ALLOWANCE MAILED		+110	CLAIMS ALLOWED				
		Assistant Examiner	Total Claims		Print Claim for D.G		
ISSUE FEE			DRAWING				
	Date Paid	†	Sheets Drwg.	Figs.Drwg	. Print Fig.		
Amount Due	Date Faid		4	11	//		
		Primary Examiner					
TERMINAL		PREPARED FOR ISSUE	Application Examiner				
	DISCLAMER	WARNING: The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368, Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.					
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